Recruitment for the post of Assistant Engineer (IT) under PHE Department

S Y L L A B U S
(Degree standard)

Total Marks: 200
Time: 2 (two) hours

Section-A: General studies   *Full Marks:* 100 Marks
(50 Multiple Choice Objective Type Questions)

  i)   Current affairs of last one & half years, particularly of Assam.
  ii)   History of Assam & India.
  iii)   World Geography including India & Assam.
  iv)   Indian Economy, Indian National Movement and Role of Assam.
  v)   Role and Impact of Science and Technology in India.
  vi)   Indian Polity, Political System in India.
  vii)   Culture of Assam & India.

Section-B: Information Technology   *Full Marks:* 100 Marks
(50 Multiple Choice Objective Type Questions)

1. **Data Structures and Algorithms:**

    Time and Space analysis of Algorithms – Order Notations. Linear Data Structures : Sequential representations – Arrays and Lists, Stacks, Queues, Strings; Link Representations – Linear linked lists, Circular linked lists, Doubly linked lists; Applications. Recursion – Design of Recursive Algorithms, Tail Recursion. Nonlinear Data Structures : Trees – Binary Trees, Traversals and Threads, Binary Search Trees, Insertion and Deletion algorithms, Height Balanced Trees and Weight Balanced Trees, B-trees, B+ trees, Application of trees; Graphs – Representations, Breadth-first and Depth-first Search. Hashing – Hashing Functions, Collision Resolution Techniques. Sorting and Searching Algorithms : Bubble sort, Selection sort, Insertion sort, Quick sort, Merge sort, Heap sort, Radix sort. File Structures: Sequential and Direct Access, Relative files, Indexed files, B+ tree aas index, Multi-index files, Hashed files.

2. **Computer Architecture and Organization:**

    Evolution of Computer: Introduction, different generations till the present time. Basic structure of a computer. Design Methodology: Components and design techniques at gate level, resistor level and processor level. Processing Unit of a Computer.

Processor organization: Number formats. Instruction formats, instruction types. Fixed point arithmetic, addition, subtraction, division and multiplication. ALU: Organization floating point arithmetic, arithmetic processor. Control Unit: Instruction sequencing and interpretation. Control unit design. Memory Organization: Types of memories. Memory device characteristics. RAM organization. Memory hierarchies. Cost and performance Virtual memories. High speed memories like caches. Parallel Processing: Introduction and types of parallel processors with performance considerations. Pipe-line processors and multiple processors.

3. **Operating Systems:**

   Process Management: Process, thread and scheduling algorithms. Concurrent process. Issues related to concurrent processes like functionality, mutual exclusion, synchronization, deadlock and inter-process communication primitives like semaphores and the implementation using machine primitives. Deadlock detection, prevention and avoidance. Memory Management Allocation, protection, hardware support, paging and segmentation. Demand paging and virtual memory. File management Naming, file operation and their implementation. File systems Allocation, free space management, directory management and mounting. File system protection, security, integrity, reliability, device independence. I/O management Device drivers, disk scheduling, block I/O and character I/O. Examples of operating systems UNIX, DOS and WINDOWS NT.

4. **Digital Systems:**

   Number representation: Signed magnitude, One's and two's complement numbers. Binary Arithmetic: Addition, subtraction, multiplication and division. Fixed and floating point arithmetic. Boolean Algebra and switching circuits Boolean algebra, Boolean expressions, logic functions, SOP and POS, function minimization - Carnaugh map and algorithms. Logic gates. Design and analysis of combinational circuits, address generation, code converters, parity generator. Sequential circuits. Flip-flops, counters, registers, decoders, encoders, multiplexers. Logic families. TTL, CMOS and ECL. RAM, ROM, E-PROM, EEPROM, PAL, PLD and PGA. Schmitt trigger and timing circuits. Current trends in digital design ASIC, FPGA and CPLD.

5. **Database Management Systems:**

   Introduction, Data Models Relational Model, Relational Algebra & Relational Calculus, SQL and other relational query languages, Relational Database Design,

Query Processing & Organization File and File Management System, Object Oriented Databases. Concurrency Control and Recovery. Distributed DBMS.

6. **Computer Networks:**

Network Basics: Evolution of computer networks; Network Models, Network Media, LAN, MAN and WAN, needs and goals of networking topology, network architecture, need for protocols, OSI Reference Model, layer services, primitives and service access points Data link layer: Framing, HDLC, PPP, sliding window protocols, medium access control, Token Ring, Wireless LAN; Virtual circuit switching: Frame relay, ATM; Network Layer: Internet addressing, IP, ARP, ICMP, CIDR, routing algorithms (RIP, OSPF, BGP); Transport Layer: UDP, TCP, flow control, congestion control; Introduction to quality of service; Application Layer: DNS, Web, email, authentication, encryption.

7. **Design and Analysis of Algorithms:**

Review of basic data structures such as stacks, queues, linked lists, trees and graphs. Concepts in algorithm analysis, asymptotic complexity. Domain independent algorithm design techniques such as divide and conquer, greedy method, dynamic programming, backtracking, branch and bound. Examples of above techniques from sets, graphs, text processing, internal and external sorting, height balanced trees, B-trees, hashing algorithms, dynamic storage allocation and garbage collection. Lower Bound theory and NP-hard problems.

Principal Controller of Examinations,
Assam Public Service Commission,
Jawaharnagar, Khanapara, Guwahati-22

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